WHAT IS CLAIMED IS:

A circuit comprising:

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2 a comparator; 3 a flip flop coupled to an output of the comparator; 4 a fixed off time/counter unit (FOTCU) coupled to the flip flop, the FOTCU containing 5 circuitry to generate a signal for a specified amount of time and to reset itself once the specified 6 amount of time expires; and 7 a gate having a first input coupled to the FOTCU and a second input coupled to an output 8 of the comparator, the gate to control the propagation of the output of the comparator when a 9 signal generated by the FOTCU is in a first state. 1 2. The circuit of claim 1, wherein the flip flop comprises an S-R flip flop, and wherein the 2 output of the comparator is coupled to an S input of the flip flop. 1 3. The circuit of claim 1, wherein the FOTCU has as an input a reference clock operating at 2 a known frequency, and wherein, when the flip flop asserts an active signal value on its output, 3 the FOTCU begins to generate the signal. 1 4. The circuit of claim 3, wherein, after the specified amount of time expires, the FOTCU 2 asserts an active signal on a finish signal line to clear the flip flop, and wherein when the flip flop 3 is cleared, the FOTCU stops generating the signal. 1 5. The circuit of claim 4, wherein the flip flop comprises an S-R flip flop, and wherein the

The circuit of claim 1, wherein the gate comprises a negative-or (NOR) logic gate.

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finish signal line is coupled to a R input of the flip flop.

1	7.	The circuit of claim 1, wherein the FOTCU counts a number of clock pulses to determine
2	the expiration of the specified amount of time.	

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- 1 8. A hysteretic controlled switch regulator comprising:
- a switch and filter unit (SFU) having an input coupled to an input voltage and an output
- 3 coupled to a load, the SFU containing circuitry to convert a direct current (DC) voltage with
- 4 ripple into a stable DC output voltage;
- 5 a comparator coupled to the SFU, the comparator to compare an output voltage generated
- 6 by the SFU with a reference voltage; and
- 7 a fixed off time unit (FOT) coupled to the comparator and the SFU, the FOT containing
- 8 circuitry to affect the operation of the SFU.
- 1 9. The hysteretic controlled switch regulator of claim 8, wherein the FOT comprises:
- a flip flop coupled to an output of the comparator;
- a fixed off time/counter unit (FOTCU) coupled to the flip flop, the FOTCU containing
- 4 circuitry to generate a signal for a specified amount of time and to reset itself once the specified
- 5 amount of time expires; and
- a gate having a first input coupled to the FOTCU and a second input coupled to an output
- 7 of the comparator, the gate to control the propagation of the output of the comparator when the
- 8 signal generated by the FOTCU is inactive.
- 1 10. The hysteretic controlled switch regulator of claim 9, wherein the signal generated by the
- 2 FOTCU disables the conversion of the input voltage with ripple into the stable DC output
- 3 voltage.

- 1 11. The hysteretic controlled switch regulator of claim 8, wherein the SFU comprises:
- a switch coupled to the input voltage, the switch to enable the conversion of the input
- 3 voltage into the stable DC output voltage when closed; and
- a filter coupled to the switch, the filter to eliminate high frequency components.
- 1 12. The hysteretic controlled switch regulator of claim 11, wherein the switch is an N-type
- 2 metal oxide semiconductor (NMOS) transistor.
- 1 13. The hysteretic controlled switch regulator of claim 11, wherein the filter comprises a low-
- 2 pass filter.
- 1 14. The hysteretic controlled switch regulator of claim 13, wherein the filter comprises:
- an inductor having a first terminal coupled to the switch and a second terminal coupled to
- 3 the load; and
- 4 a capacitor having a first terminal coupled to the second terminal of the inductor and a
- 5 second terminal coupled to an electrical ground.
- 1 15. The hysteretic controlled switch regulator of claim 8, wherein the comparator asserts an
- 2 active value on its output when the output voltage is greater than the reference voltage.
- 1 16. The hysteretic controlled switch regulator of claim 8, wherein when the SFU is enabled,
- 2 the output voltage will rise until the output voltage exceeds the reference voltage, and wherein
- 3 when the output voltage exceeds the reference voltage, the comparator asserts an active value on
- 4 its output and the FOTCU generates a signal to disable the SFU.
- 1 17. The hysteretic controlled switch regulator of claim 16, wherein a magnitude of the load
- 2 will determine how rapidly the output voltage rises.

- 1 18. The hysteretic controlled switch regulator of claim 17, wherein when the load is small in
- 2 magnitude, the output voltage will rise slowly.
- 1 19. The hysteretic controlled switch regulator of claim 8, wherein the input voltage is a
- 2 rectified voltage produced by an alternating current (AC) adaptor.

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